IN THE SPECIFICATION:

Please amend paragraph number **[0007]** as follows:

[0007] United States Patent ~~5,818,197~~ 5,818,107 issued to Pierson et al. teaches an integrated circuit package that utilizes metallization features, located at opposite edges of each chip, to attach a stack of chips to a substrate. The chips are bonded together through their metallization features to form a chip stack, which is then bonded to the substrate. The thickness of the metallization features, in addition to the bonding material used, provides a "stand off" or separation between chips. This separation adds to the overall thickness of the integrated circuit package, making it incompatible for use in electronic devices that require small semiconductor packages.

Please amend paragraph number **[0034]** as follows:

[0034] As is illustrated in drawing FIG. 5 (~~bond pads~~electrical contacts **20**, vias **24**, and substrate **22** not shown), the present invention also relates to a method of packaging semiconductor dice in a high density arrangement. The semiconductor dice are packaged by providing at least one semiconductor die **12**, a flexible interposer **10**, and a substrate **22**. The interposer **10** is folded around and attached to the semiconductor dice **12**. The interposer **10** has a first surface **16**, a second surface **18**, and vias **24** that extend through the interposer **10** from the first surface **16** to the second surface **18**. The first surface **16** includes electrical contacts **20**. The semiconductor dice **12** are attached to the interposer **10** through bond pads **26** on the active surface of the semiconductor die **12** to form intermediate packaging structure **28**. Intermediate packaging structure **28** is then attached to substrate **22** through the electrical contacts **20** to form a high density semiconductor package **14**. This attachment also results in electrical communication between the semiconductor die **12** and the substrate **22**. In a high density semiconductor package **14** containing one semiconductor die **12**, the interposer **10** is folded around the semiconductor die **12** so that at least three sides of the semiconductor die are surrounded, as is illustrated in drawing FIG. 2 (vias and substrate not shown). In a high density semiconductor package **14** containing two semiconductor dice **12**, the interposer **10** surrounds at

least two sides of each semiconductor die **12**, as is illustrated in drawing FIG. 3 (vias and substrate not shown). Illustrated in drawing FIG. 5 (bond pads, vias, and substrate not shown) is that the interposer **10** weaves in a serpentine fashion between semiconductor dice **12** stacked in groups of two when a high density semiconductor package **14** containing more than two semiconductor dice **12** is desired. Additionally, electrical contacts **20** may be applied to a top surface **30** of the package **14**, as is shown in drawing FIG. 6 (bond pads, vias, and substrate not shown), so that the package **14** can be attached to other semiconductor devices, depending on the desired application.